Course Outcomes Guide (COG)

Course Title: EGR 210 Digital Logic Design **Date:** December 19, 2017
Course Team: Ed Sigler

Expected Learning Outcomes (Lecture and Lab)

1. Apply knowledge of mathematics, science, and engineering.
2. Apply Boolean algebra techniques to digital circuit analysis.
3. Use the techniques, skills, and modern engineering tools necessary for successful practice.
4. Design and conduct experiments and interpret analysis results.

Assessment
The assessment for the course common mid-term and final exams administered to all sections of EGR 208. The problem types and complexity are maintained as constant as possible across semesters to track per class variations. Students are assessed on the following capabilities:

1. Learn and apply Boolean Algebra to logic circuits
2. Analyze and design combinational logic circuits
3. Analyze and design logic circuits with encoders, decoders, multiplexors, etc.
4. Investigate Latches and Flip-Flops
5. Analyze and design register and synchronous sequential logic circuits.
6. Investigate Programmable Logic Devices (PLDs) and Programmable Logic Arrays (PLAs)
7. Laboratory experiments in basic, combinational and sequential logic circuits

Validation
Learning outcomes are assessed through homework problems, exams, lab experiments and lab exams (including individual practicals). Common questions for each exam are given to each section of the course. Data collected from these exams will be used to identify areas of weakness and to adjust instruction accordingly.

Results
FA 2017 is the first run of EGR 210 at HCC. Significant time and energy were devoted to development of lab activities that would complement and emphasize material covered in lectures. The labs are structured for materials to be covered in lecture prior to coverage as part of lab experiments.

The expected learning outcomes were met via instruction and validation via in-class assignments, exams, lab reports and lab exams. The initial class size was 4 students. No deficiencies were noted in coverage or student learning.

Major Findings
Fall 2017:

- Student performance on exams was above that expected. Likely due to more individualized instruction with a class size of 4.

Follow-up
The course will be adjusted to reflect the degree of difficulty for material. Resistive network coverage will be shortened to allow for deeper coverage of RCL circuit response, phasors, transformers and filter responses.

Budget Justification
No additional budget is required for this class.

Course: EGR 210 **SLOA Data** **Faculty Team: E. Sigler**

	FA 2017	SP 2018	FA 2018	SP 2019	FA 2019	SP 2020	FA 2020	SP 2021
# Active students	4	N/A		N/A		N/A		
%W	0							
*# walk-away Fs No final exam/grade = F	0							
% Success (A,B,C)	100%							
Common Comprehensive Final Exam Score Average	77.1%							
Mean course grade	3.5**							
Item Analysis **Weakest Content Areas**	Sum of Product to Product of Sums conversions							

*% Walk-away Fs = Did not take the final exam and received a grade of F.

** FA 2017 was the initial course offering with 4 students